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SuperCDMS Detector Readout Cryogenic Hardware

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Abstract. SuperCDMS employs 1-inch thick germanium crystals operated below 50mK in a dilution cryostat. Each detector produces ionization and phonon signals. Ionization signals are amplified by JFETs operating at 150K within an assembly mounted on the 4K cryostat stage. These high impedance signals are carried to the FETs by superconducting "vacuum coaxes" which minimize thermal conductivity, stray capacitance, and microphonics. Transition edge sensors produce low-impedance phonon signals, amplified by SQUID arrays mounted on a 600mK stage. Detectors are mounted in a six-sided wiring configuration called a "tower", which carries signals from 40mK to 4K. A flex circuit 3 meters in length carries amplified signals for each detector from 4K to a vacuum bulkhead. We describe the methods used to support the detectors, wiring and amplifier elements at various thermal stages, minimizing electrical noise and thermal loads.

Keywords: CDMS, SuperCDMS, Dark Matter, Cold Hardware.

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INTRODUCTION

The Cryogenic Dark Matter Search (CDMS) and SuperCDMS projects employ germanium detector crystals cooled below 50mK. Each detector (one CDMS design is shown in Fig. 1) is instrumented with two charge collection electrodes and four transition edge sensor arrays. Measuring the ratio of ionization to phonon energy enables CDMS detectors to distinguish different particles. The “cold hardware” is defined as all assemblies within the cryostat. This includes physical support, detector packaging, interconnections, and biasing and preamplification components [1].

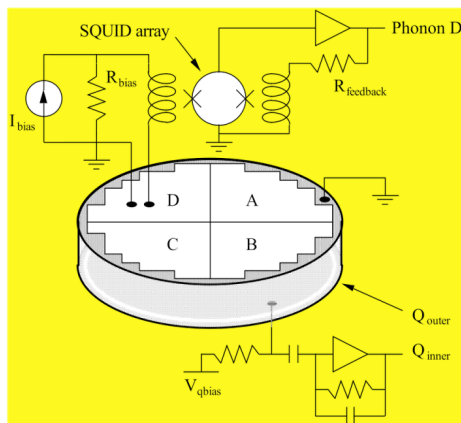


FIGURE 1. A CDMS detector with cold hardware components. Amplifier symbols indicate room temperature electronics. “Quad” phonon sensor geometry shown.

CHALLENGES

CDMS detectors operate at very low temperatures, requiring the cold hardware to span a range from 10mK to 300K. This necessitates careful consideration of component power dissipation and thermal loading by wires. Signal sensitivity determines experiment thresholds, so care has to be taken to minimize intrinsic component noise and to avoid noise induced by microphonic or electromagnetic pickup. To minimize radioactive backgrounds, the experiment is operated in the Soudan mine at a depth of 2,341 feet. To further reduce backgrounds, the detectors are surrounded by lead and polyethylene shielding, requiring a signal path 5 meters long between preamplifier components and the room temperature electronics. All cold hardware is contained within the shields, so materials used must be intrinsically low in backgrounds.

Ionization and phonon signals produced on an event-by-event basis each require unique considerations. The ionization signals are preamplified by InterFET IF4501 JFETs. The high impedance gate wire of the JFET is sensitive to noise pickup, and

measurement noise is proportional to total input capacitance. These considerations necessitate mounting the JFETs within inches of the detectors, even though each JFET dissipates a few milliwatts and must be operated above 100K to prevent freezeout.

Phonon signals are produced by low impedance (~ 0.2 Ohm) tungsten transition edge sensor (TES) arrays, and are preamplified by a SQUID array [2]. The interconnect resistances must be kept low to avoid thermal noise and reduction in sensitivity. Each Nb-based SQUID array dissipates microwatts and must be operated well below its superconducting transition temperature of 9.3K. The SQUIDs must also be well shielded from both DC and AC magnetic fields to maximize SQUID signal-to-noise.

CDMS cold hardware was originally designed for NTD-Ge phonon sensors, using JFETs for both charge and phonon readouts. When faster athermal phonon TES sensors replaced the NTDs in the late 1990's, tradeoffs were made to avoid redesign of large portions of the hardware. This avoided significant delays, but resulted in a more complex design than one started ab initio.

MECHANICAL AND THERMAL

Figure 2 shows a cross section of the SuperCDMS cold hardware. The core of the cold hardware design is the six-sided “Tower”, a mechanical assembly used to transport the detector wires from 10mK to 4K. Using thermal intercepts at 50mK, 600mK and 4K minimizes heat load onto the detector stage. The copper floors of the tower are thermally isolated and mechanically supported by thin walled graphite tubes. Flexible annealed copper links are used to connect each Tower floor to a corresponding cryostat stage. Superconducting NbTi wires are strung under tension to compensate for thermal contraction of the graphite. Heat sink boards at each stage work with the NbTi wires to form a thermal divider that shunts heat to each temperature level (“floor”) while impeding flow between floors. Copper cladding on the wires provides solderability at the heat sinks but is chemically removed between stages to provide thermal isolation.

Detectors are supported beneath the “10mK” tower floor, centered vertically within the cryostat. Five 1-inch thick detectors are held within modular detector housings stacked up between two 1cm veto detectors. “Side Coax” assemblies bring connections from each detector assembly to one face of the tower. “SQUET” assemblies plug into the tower 4K floor to hold the SQUID and FET preamplifier components. A 3 meter “Stripline” flex circuit (not shown) plugs into the SQUET and carries preamplified signals to a 300K vacuum bulkhead feedthrough connector.

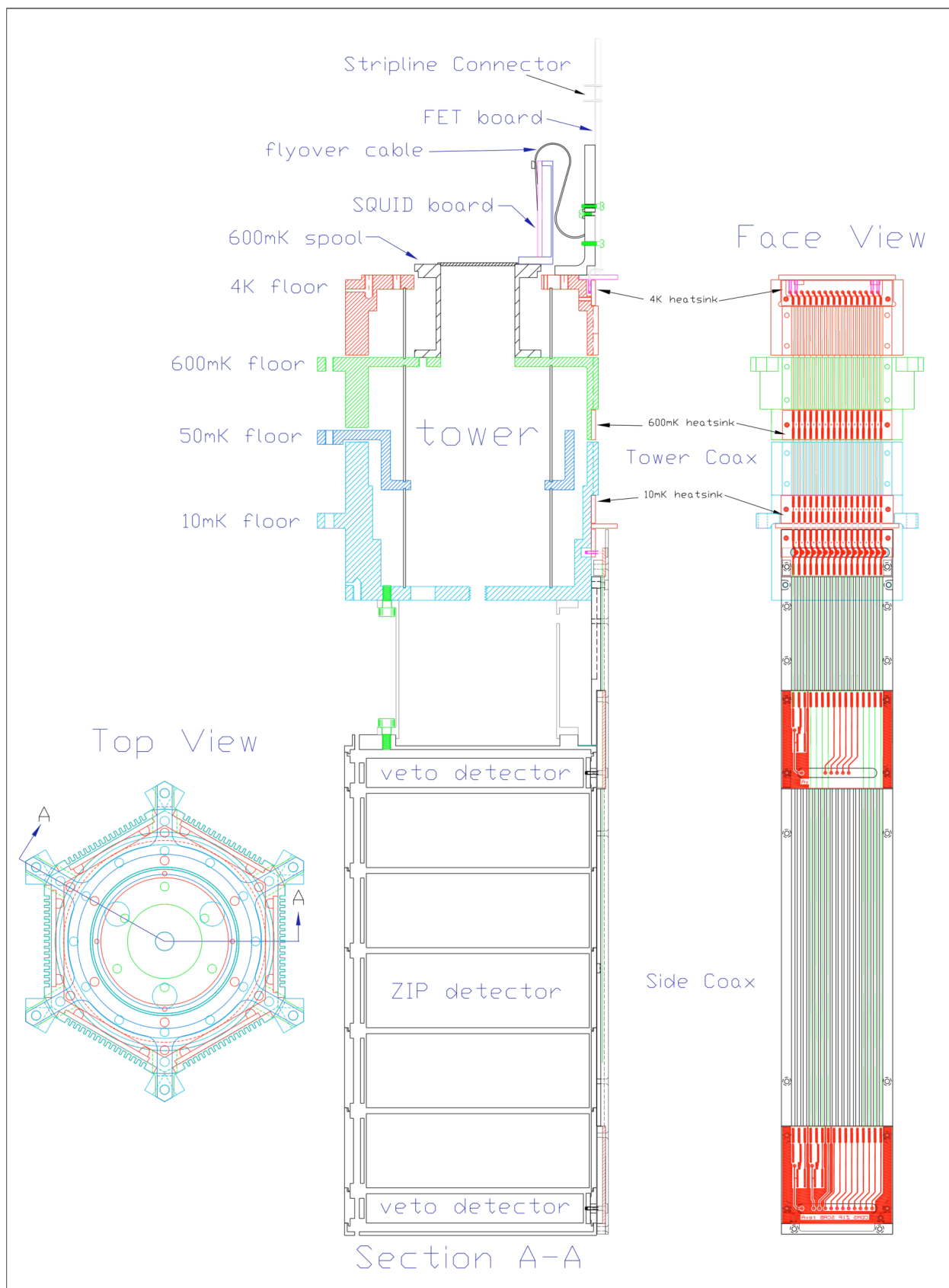


FIGURE 2. SuperCDMS detector stack

RADIO PURITY

Oxygen-free high conductivity (OFHC) copper is the primary material used in the cold hardware due to high thermal conductivity and low intrinsic radioactivity. Parts are acid etched to remove surface contaminants. Circuit boards are fabricated from copper-clad polyimide to avoid the intrinsic radioactivity of fiberglass. Solder is custom made from low activity lead. Assemblies are constructed and stored under clean room conditions to minimize contamination.

ELECTRICAL DESIGN

The electrical design can be divided into two sections, ionization channels and phonon channels. The “SQUET” assembly consists of two circuit cards. The SQUID card holds phonon preamplifier SQUIDs operating at 600mK, while the FET card holds ionization preamplifier JFETs operating at 150K. The two cards are approximately one inch apart.

Ionization Channels

The 40M Ω charge biasing and feedback resistors are mounted on the Side Coax adjacent to the detector at base temperature to minimize Johnson noise. The high impedance gate wire must be routed several inches from the detector to each JFET within the FET card mounted at 4K. This wire is enclosed within copper “vacuum coax” channels on the Tower and Side Coax. Absence of insulator minimizes microphonic noise caused by triboelectric effects. Biasing the FET gate at zero volts prevents microphonics caused by any motion of the gate wire within an electric field.

The FET card contains the “FET window”, a flex circuit that allows the JFETs to operate at 150K within the 4K SQUET assembly. The FET window is suspended within the “FET gusset”, a copper enclosure that contains and absorbs IR emitted by the JFETs. Various IR shields further prevent IR leakage into the detector space. The FET window is a 0.001” thick polyimide flex printed circuit that employs 1um thick copper conductors a few cm long to provide a specific thermal impedance. A resistor is mounted on the window near the JFETs to preheat them to operating temperature. Once the JFETs are operating, internal power dissipation combined with the thermal impedance of the window maintains them at 150K. The Stripline carries the bias, feedback, JFET drain, and source connections to the 300K electronics.

Phonon Channels

The TES signal and return lines are also routed in vacuum coaxes between the detector and the FET card. From the FET card they pass through a superconducting “Flyover” twisted pair ribbon cable to the SQUID card mounted at 600mK. The Flyover cable is an epoxy and polyimide lamination containing twisted pairs of insulated CuNi clad NbTi wires. The CuNi cladding allows the wires to be soldered while providing adequate thermal isolation. The NIST SQUID array chips are mounted at the SQUID card on Nb foil, which is used to pin any ambient magnetic fields, already reduced by magnetic shielding at 300K surrounding the detector space. Four SQUID arrays are used to amplify current signals from the four TES phonon sensors on each detector. Phonon bias inputs and SQUID output and feedback signals are also routed within the flyover cable to the FET card, where they are brought to the 300K electronics by the Stripline cable.

It would seem more straightforward to mount the SQUIDs on the 600mK tower face, and route the TES signals using twisted pairs instead of vacuum coaxes. When the TES sensor technology replaced the original NTDs, however, the tower design and test was complete and several had been constructed. A decision was made to retrofit the existing design. The SQUET assembly provided a conveniently modular replacement for the previous FETs-only card, and the TES signal and return lines were simply left in the vacuum coaxes.

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